Listing of Claims:

1. (Currently Amended) A ~~SDH~~ synchronized digital hierarchy (SDH) test apparatus ~~for substituting a part of payload of received SDH data with a desired data and transmitting~~, comprising:

~~a~~ an Rx ~~SOH~~ section overhead (SOH) processor for performing frame detection of ~~said~~ received SDH data;

~~a~~ an Rx ~~AU~~ administrative unit (AU) processor for extracting AU data composed of an AU pointer ~~of~~ and a payload from data processed by said Rx SOH processor ~~and payload~~, and for detecting an information leading head position designated by said AU pointer;

a Tx AU processor for generating AU data ~~wherein~~ in which a part of the payload of AU data extracted by said Rx AU processor is substituted with a desired data;

a Tx SOH processor for generating a new SDH data with the AU data generated by said Tx AU processor and the data from said Rx SOH processor and transmitting the new SDH data;

a FIFO memory installed between said Rx AU processor and said Tx AU processor, for sequentially storing ~~sequentially~~ payload data of AU data extracted by said Rx AU processor and outputting to said Tx AU processor in ~~the~~ an order of memorization; and

an AU pointer processor for outputting an AU pointer adjusting ~~the~~ a number of data in said FIFO memory, allowing said Tx AU processor to read in the payload of AU data, after a time lag ($\Delta T2 + \Delta T4$) of an information leading head position of the payload generated by ~~the~~ processing of AU data by said Rx AU processor and said Tx AU processor, by extracting the number of data in said FIFO memory,

wherein said Tx AU processor is ~~composed~~ adapted to read out the payload of AU data from said FIFO memory, generate AU data, and output to said Tx SOH processor so that said information leading head position is at ~~the~~ a position designated by ~~the~~ an AU pointer value output from said AU pointer processor.

2. (Currently Amended) ~~A~~ The SDH test apparatus according to claim 1, further comprising:

~~a~~ an Rx ~~TU~~ tributary unit (TU) processor for extracting TU data ~~by~~ from the data processed by said Rx AU processor;

a second FIFO memory for successively storing ~~successively~~ the TU data extracted by said Rx TU processor;

a Tx TU processor for performing transmission TU processing for TU data output from said second FIFO memory in ~~the~~ an order of memorization; and

a TU pointer processor ~~composed~~ which is adapted to decide ~~the~~ a TU pointer anticipating ~~the~~ an information leading head position shifting due to ~~the~~ a processing time of the TU data by the Rx TU processor and the Tx TU processor ~~, the~~ and a delay time ~~to maintain~~ for stably maintaining a data storage state of said second FIFO memory ~~data storage state stable~~.

3. (Currently Amended) A ~~SDH~~ synchronized digital hierarchy (SDH) test method ~~for substituting a part of payload of received SDH data with a desired data and transmitting~~, comprising ~~the steps of~~:

Rx ~~SOH~~ section overhead (SOH) processing including frame detection of ~~said~~ received SDH data;

Rx ~~AU~~ administrative unit (AU) processing including extraction of AU data composed of an AU pointer ~~of~~ and a payload from data processed by said Rx SOH processing and payload, and detection of ~~the~~ an information leading head position designated by said AU pointer;

Tx AU processing including generation of AU data ~~wherein~~ in which a part of the payload of AU data extracted by said Rx AU processing is substituted with a desired data;

Tx SOH processing including generation of a new SDH data with the AU data generated by said Tx AU processing and the data ~~by~~ from said Rx SOH processing and transmission thereof;

sequentially storing ~~sequentially~~ the AU data extracted by said Rx AU processing between said Rx AU processing and said Tx AU processing in a FIFO memory and transmitting to said Tx AU processing in ~~the~~ an order of memorization; and

AU pointer processing for outputting an AU pointer adjusting ~~the~~ a number of data in said FIFO memory, allowing said Tx AU processing to read in the payload of AU data, after a time lag ($\Delta T2 + \Delta T4$) of an information leading head position of the payload generated by the processing of the AU data by said Rx AU processing and said Tx AU processing, by extracting the number of data in said FIFO memory,

wherein said Tx AU processing ~~is composed to read~~ includes reading out the payload of AU data from said FIFO memory, ~~generate~~ generating AU data, and ~~output~~ outputting to said Tx AU processing so that said information leading head position is at ~~the~~ a position designated by ~~the~~ an AU pointer value output from said AU pointer processing.

4. (Currently Amended) ~~A~~ The SDH test method according to claim 3, further comprising the steps of:

Rx ~~TU~~ tributary unit (TU) processing for extracting TU data ~~by~~ from the data processed by said Rx AU processing;

successively storing ~~successively~~ the TU data extracted by said Rx TU processing in a second FIFO memory;

Tx TU processing for performing Tx TU processing for TU data output from said second FIFO memory in ~~the~~ an order of memorization; and

TU pointer processing to decide ~~the~~ a TU pointer anticipating ~~the~~ an information leading head position shifting due to ~~the~~ a processing time of the TU data by the Rx TU processing and the Tx TU processing ~~, the~~ and a delay time ~~to maintain~~ for stably maintaining a data storage state of said second FIFO memory ~~data storage state stable~~.